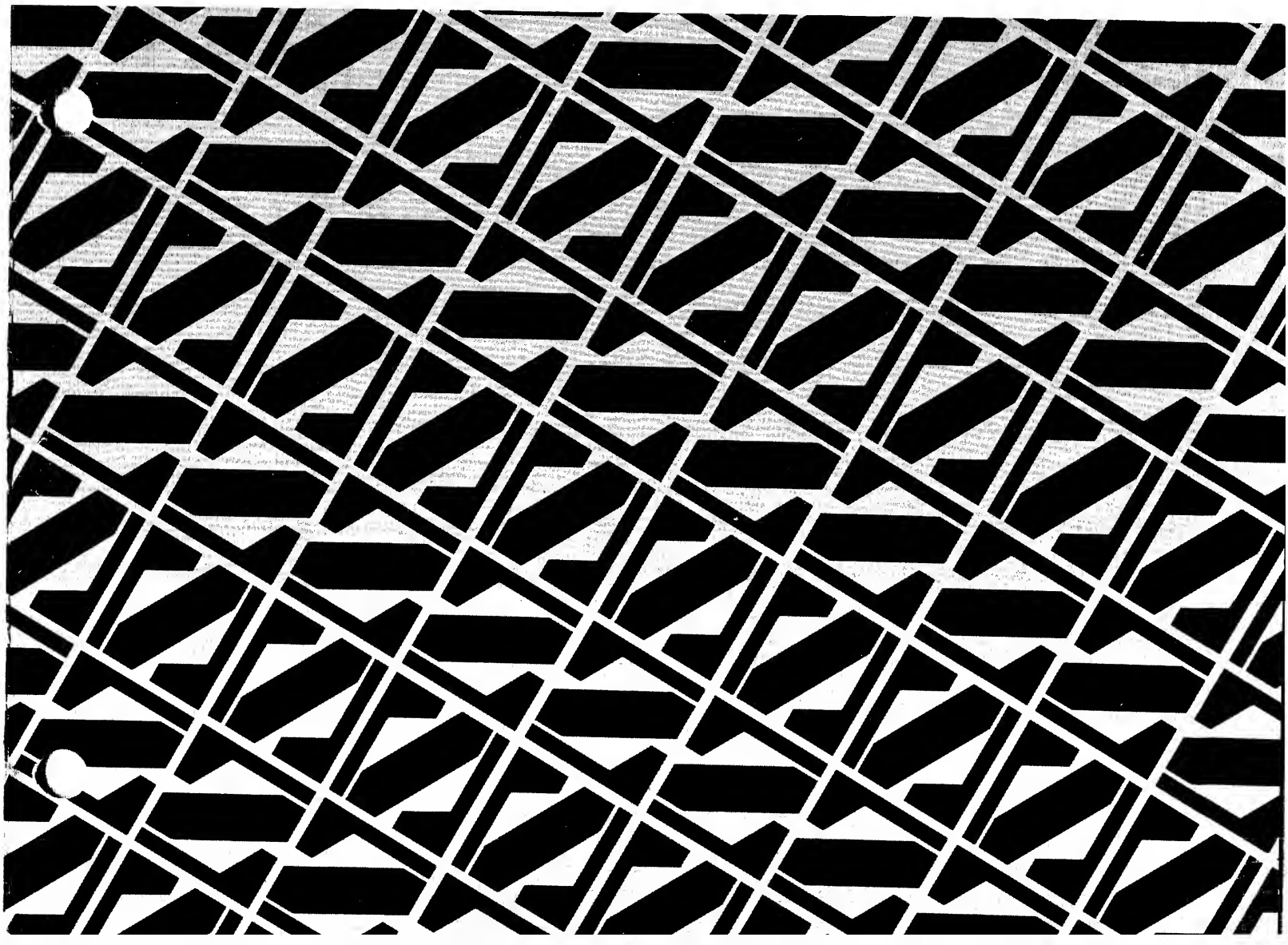
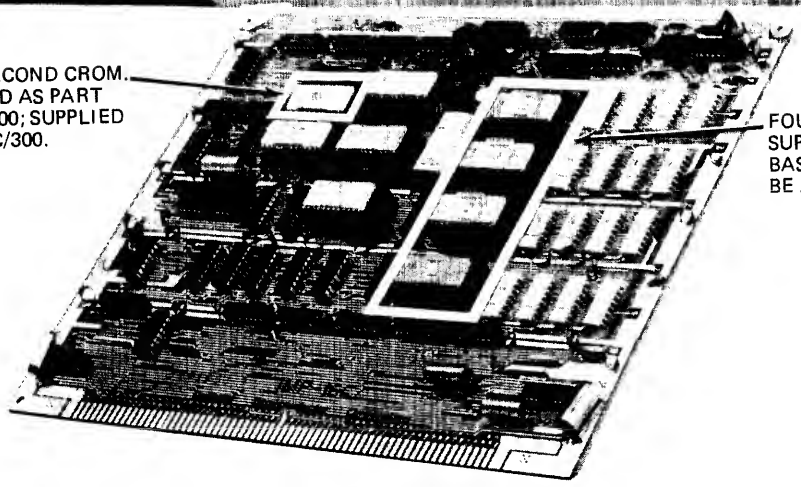
National Semiconductor
Order No. IMP-16P/936A
Pub. No. 4200036A

IMP-16C/200
IMP-16C/300
Microprocessors
IMP-16P
Microcomputer
Product Descriptions



IMP-16P MICROCOMPUTER



OPTIONAL SECOND CROM. NOT SUPPLIED AS PART OF IMP-16C/200; SUPPLIED WITH IMP-16C/300.

FOUR PROMs NOT SUPPLIED AS PART OF BASIC IMP-16Cs. MAY BE ADDED AS OPTIONS.

IMP-16C MICROPROCESSOR

1.0 INTRODUCTION

The IMP-16 microcomputer family is available in a variety of configurations: as a system (IMP-16P), as a CPU card (IMP-16C), and as an MOS-component kit. The configuration that is most attractive to a given user depends upon a variety of factors, which may change over the life of the system manufacturer's product. An important advantage of the availability of these different configurations of the IMP-16 is the option of changing the configuration in response to changing conditions. For example, the system manufacturer may initially procure the IMP-16P as a stand-alone system in order to expedite software development and to permit rapid assembly of models for field trial. Later, it may be more economical to purchase subassemblies that are packaged in an enclosure customized for the application. When production quantities warrant, the system manufacturer may purchase at the semiconductor component level. Thus, the manufacturer may optimize both his development and production phases due to the versatility of the IMP-16 design and options.

The IMP-16C/200 is a pin-compatible version of the earlier IMP-16C card, with the layout changed to accommodate a second CROM (Control Read Only Memory). This CROM may be supplied with an extended instruction set, as described later in this brochure, or the second CROM can be customized for special applications. The IMP-16C/200 is supplied with only one CROM (programmed for the basic instruction set) and with an empty CROM socket. The IMP-16C/300 has two CROMs, the second CROM programmed for the extended instruction set and inserted in the second CROM socket. This is the only difference between the two cards.

The IMP-16P microcomputer is also available as either the IMP-16P/200 or the IMP-16P/300. These two versions differ only in that the IMP-16P/200 contains the IMP-16C/200 card (one CROM), whereas the IMP-16P/300 contains the IMP-16C/300 card (two CROMs). This is the only difference between the two microcomputers.

Descriptions that follow pertain to both versions of the IMP-16C and the IMP-16P unless otherwise noted.

IMP-16C/200 AND IMP-16C/300 MICROPROCESSOR CARDS

An IMP-16C Integrated Microprocessor is a flexible, low-cost, self-contained 16-bit parallel processor on a card. It is designed for computer-oriented equipment such as data terminals, test systems, communications equipment, machine tool controllers, process control systems, and peripheral device controllers. With an IMP-16C, the system designer has a proven, totally debugged processor that he may customize to his immediate application by programming rather than by "hard-wiring." This technique can yield considerable savings, both in terms of money and developmental time – in contrast to costly inhouse-developed processors or controllers that use hard-wired logic.

IMP-16P MICROCOMPUTER SYSTEM

The IMP-16P microcomputer is a prototyping tool designed to aid the microprocessor user in developing hardware and software systems around the IMP-16C microprocessor cards and component sets. It includes a chassis, programmers control panel, power supplies, and one or more 4K 16-bit-word read/write memory modules, in addition to an IMP-16C card. With a Teletype®, the IMP-16P provides all equipment and software necessary for the immediate evaluation and use of the IMP-16C microprocessor cards and MOS/LSI devices. The IMP-16P is especially useful for the development of application software and equipment interfaces.

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OPERATIONAL FEATURES

Feature	IMP-16C	IMP-16P
Word Length	• 16 bits	• Same as IMP-16C
Instruction Set	• 43 in IMP-16C/200 (implemented by CPU-resident microprogram) • 60 available in IMP-16C/300 (includes 43 as for IMP-16C/200 and 17 additional instructions)	• IMP-16P/200 – same as IMP-16C/200 • IMP-16P/300 – same as IMP-16C/300
Arithmetic	• Parallel, binary, fixed point, twos complement	• Same as IMP-16C
Memory	• 256 16-bit words of read/write memory • Sockets for 512 16-bit words of semiconductor read-only memory	• 16-bit words of semiconductor memory expandable in increments of 4096 words to a maximum of 65,536 words
Addressing Modes	• Page size of 256 words • Direct and indirect modes • Base page – 256 words	• Same as IMP-16C

Feature	IMP-16C	IMP-16P
Addressing Mode (Cont.)	• Current page – 256 words • Relative to Accumulator 2 or 3* – 256 words *Indexing gives maximum range of 65,536 words in page sizes of 256 words each	• Same as IMP-16C (Cont.)
Typical Instruction - Execution Speeds	• Register-to-register addition – 4.55 μs • Memory-to-register addition – 7.7 μs • Register input/output – 10.5 μs	• Same as IMP-16C • Same as IMP-16C
Operating Speed	• 1.4 μs microcycle time	• Same as IMP-16C
Input/Output and Control	• 16-bit peripheral data input port • 16-bit memory data input port • 16-bit data output bus • 16-bit address bus • 4 general-purpose jump condition inputs • 6 general-purpose control flags • 1 general interrupt condition • 1 vectored interrupt input	• Same as IMP-16C
Input Power (at 25°C)	• +5 volts at 2.25 amperes • -12 volts at 0.51 amperes • -9 volts at 0.59 amperes (for on-card memory; may be developed from -12 volt source)	• 105 to 125 VAC at 60 Hz (220 VAC, 50 Hz optional)
Temperature	• Operating – 0 to 70°C • Storage – -20 to 100°C	• Operating – 0 to 50°C • Storage – -20 to 70°C
Humidity	• Maximum of 90% relative humidity without condensation	• Same as IMP-16C
Dimensions	• 8-1/2-by-11-inch card, 1/2-inch height	• 12-inch-high, 17-inch-wide, 24-inch-long chassis

2.0 IMP-16C/200 AND IMP-16C/300 DESCRIPTIONS

The major functional units of the IMP-16C are shown in figure 2-1 and consist of the following:

- Central Processing Unit (CPU)
- Clock Generators
- Input Multiplexer
- Data Buffer
- Control Flags
- Conditional Jump Multiplexer
- On-Card Memory
- Address Latches

The CPU consists of four Register and Arithmetic Logic Units (RALUs), a 4-bit control bus, and one or two Control and Read-Only Memories (CROMs). The RALUs and the CROMs are individual MOS/LSI devices. A RALU is a 4-bit unit, and four RALUs in parallel form a 16-bit unit. The RALUs are controlled by microinstructions stored in the CROM(s).

A system clock is available for distribution outside of the IMP-16C for synchronization of peripheral units with the IMP-16C. Thirteen addressable Control Flags are available to the user. Conditional branch conditions are selected by the Conditional Jump Multiplexer, from which they may be tested to determine if a branch should occur. Four of these jump conditions are user-specified, and can be monitored and tested by the CPU.

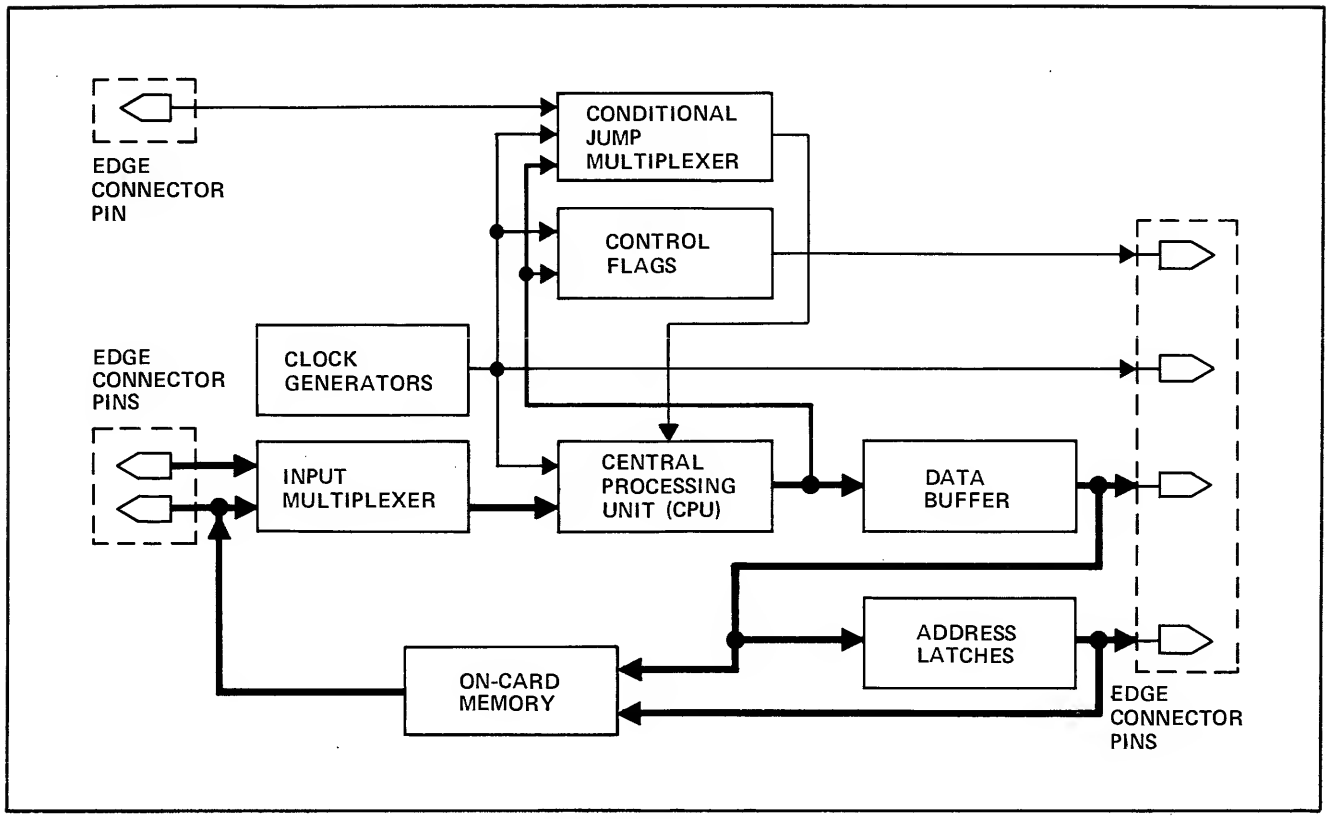


Figure 2-1. IMP-16C Major Functional Units

Buffered data are made available over a 16-bit bus to the user's peripheral devices, control panel, and add-on memory. Addresses are taken from a separate 16-bit bus.

The memory on the IMP-16C card consists of 256 16-bit words of read/write (RAM) memory and sockets for 512 16-bit words of read-only (ROM/PROM) memory. The off-card memory may be expanded in increments of 4,096 16-bit words to provide a total memory of 65,536 words.

REGISTER AND ARITHMETIC LOGIC UNIT (RALU)

The CPU module provides four 16-bit Accumulators (AC0, AC1, AC2, and AC3) for data storage (figure 2-2). Two of these (AC2 and AC3) may also be used as index registers.

Three additional registers are provided for use by the CPU and are not directly available to the programmer. These registers serve the function of Program Counter (PC), Memory Address Register (MAR), and Memory Data Register (MDR).

A last-in/first-out hardware Stack is provided in the CPU. This Stack is used to automatically save subroutine addresses and interrupt return addresses, thereby allowing several levels of nested operation. In addition, the top word of the Stack may be accessed with certain selected instructions.

Sixteen Status Flags are also provided in the CPU. These are modified individually during various CPU operations and collectively (as a 16-bit status register) by certain instructions. The flag assignments are shown in figure 2-3.

The ALU provides the capability for operating on data stored in any of the above elements. All arithmetic operations are performed using binary twos-complement arithmetic.

CONTROL READ ONLY MEMORY (CROM)

All actions of the CPU module are directed by a microprogram stored in a CROM. The microinstructions are very basic and control the actions of the CPU at a very detailed level. Moreover, they have a short execution time; this makes it practical to use a number of these microprogram-level instructions (microinstructions) to implement more-powerful instructions (macroinstructions) used by the programmer.

INSTRUCTION SET

The available IMP-16 instructions consist of both a basic 43-instruction set and an expanded 17-instruction set. The basic instructions are implemented by one Control Read-Only Memory (CROM) and the expanded instructions by a second CROM. Because the basic instructions are common to all IMP-16 microprocessors, the IMP-16P may be used to develop programs for other IMP-16 systems.

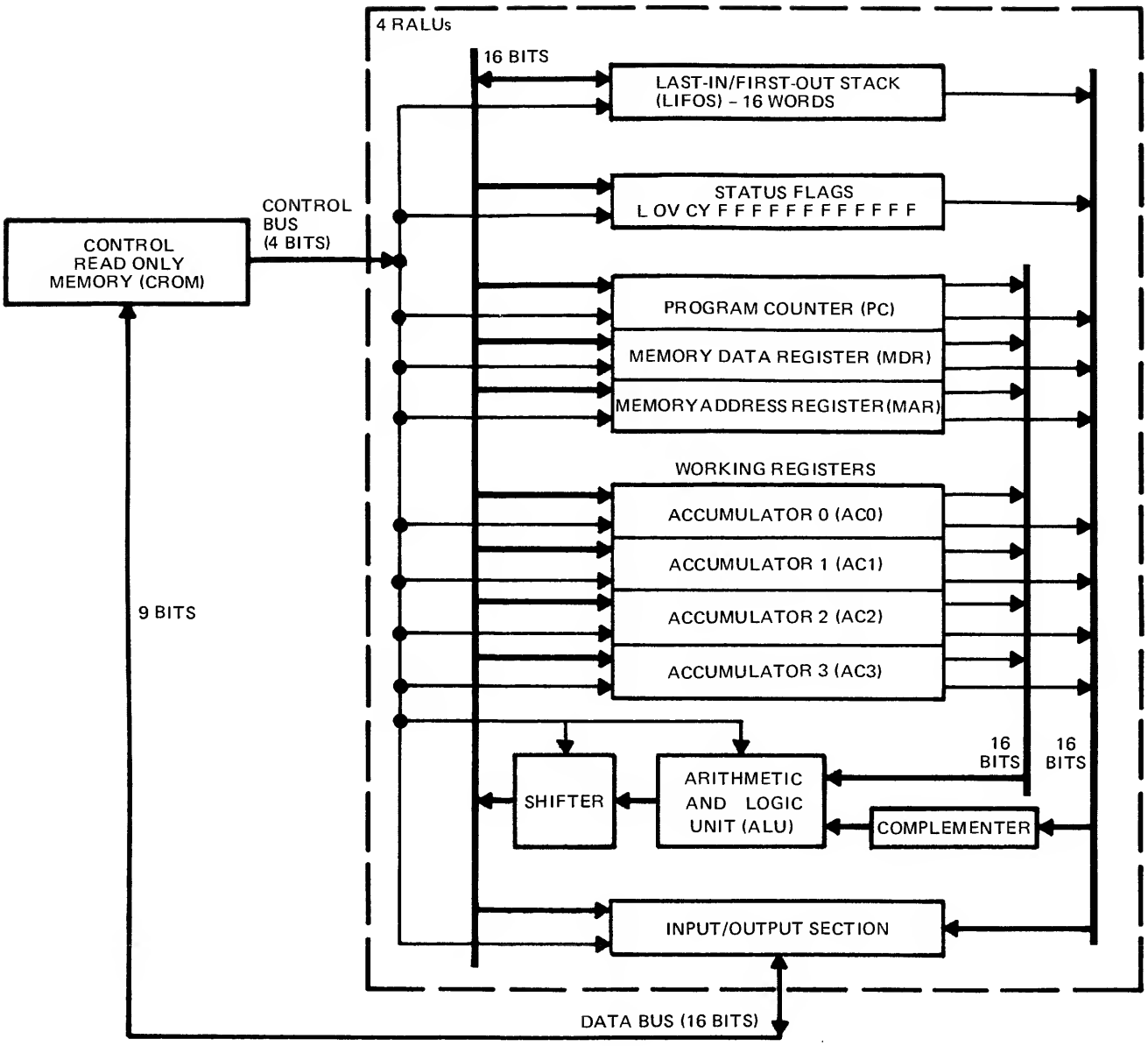


Figure 2-2. CROM and Four RALUs

Basic Instruction Set

The basic format for the memory reference instruction is shown in figure 2-4. Multiple addressing modes are possible, as specified by the value of *xr*. With the base page mode of addressing (when $xr = 0$), the memory address is determined solely by the value of the displacement field, *disp*, taken as an unsigned number from 0 to 255. When $xr = 1$, the mode of addressing is relative: the memory address is formed by adding the Program Counter contents to the value of *disp*, interpreted as a signed number from -128 to +127. With the remaining two modes of addressing, two of the four working accumulators may be used as index registers: the value of *disp* taken as a signed number is added to the contents of the chosen index register.

The *r* field specifies one of the four working accumulators that is to be used in the instruction. The operation code for the instruction is specified by the OpCode.

Other classes of instructions use modifications of the format shown in figure 2-4. A "register-to-register" class of instructions uses the *xr* value to specify a second register. A "single-register" class of instructions has the operation code field extended to six bits, with the *xr* value specifying the register. A list of the 43 basic instructions is provided in table 2-1.

Extended Instruction Set

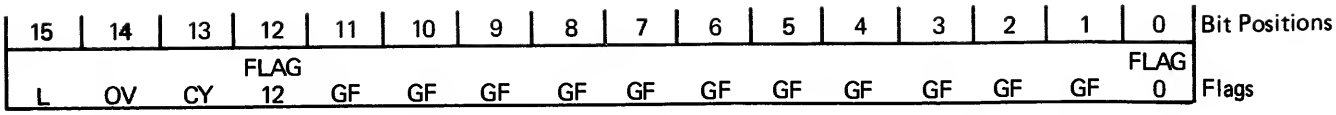
A group of 17 additional instructions is available with the IMP-16C/300. Six memory reference instructions are provided; these instructions use indexed addressing similar to the basic instruction set, except a double-word format (figure 2-5) is used (16-bit displacement field). The non-memory reference instructions (of the extended group) use a single-word format. A list of the 17 extended instructions is provided in table 2-2.

Table 2-1. IMP-16 Basic Instruction Set

Instruction	Mnemonic	Execution Cycles
Memory Reference Instructions		
Load	LD	5
Load Indirect[a]	LD	5
Store	ST	6
Store Indirect[a]	ST	8
Add	ADD	5
Subtract	SUB	5
Jump	JMP	3
Jump Indirect[a]	JMP	5
Jump to Subroutine	JSR	4
Jump to Subroutine Indirect[a]	JSR	6
Increment and Skip if Zero	ISZ	7,8 if SKIP
Decrement and Skip if Zero	DSZ	8,9 if SKIP
Skip if AND is Zero	SKAZ	6,7 if SKIP
Skip if Greater	SKG	Like Signs: 8,9 if SKIP Unlike Signs: 9,10 if SKIP
Skip if Not Equal	SKNE	6
And	AND	5
Or	OR	5
Register Reference Instructions		
Push on to Stack Register	PUSH	3
Pull from Stack	PULL	3
Add Immediate. Skip if Zero	AISZ	4,5 if SKIP
Load Immediate	LI	3
Complement and Add Immediate	CAI	3
Register Copy	RCPY	6
Exchange Register and Top of Stack	XCHRS	5
Exchange Registers	RXCH	8
Register And	RAND	6
Register Exclusive Or	RXOR	6
Register Add	RADD	3
Shift Left	SHL	4 + 3k[b]
Shift Right	SHR	4 + 3k
Rotate Left	ROL	4 + 3k
Rotate Right	ROR	4 + 3k
Input/Output, Flag, and Halt Instructions		
Set Flag	SFLG	4
Pulse Flag	PFLG	4
Push Flags on Stack	PUSHF	4
Pull Flags from Stack	PULLF	5
Register In	RIN	7
Register Out	ROUT	7
Halt	HALT	–
Transfer of Control Instructions		
Branch-On Condition	BOC	4,5 if branch
Return from Subroutine	RTS	4
Return from Interrupt	RTI	5
Jump to Subroutine Implied	JSRI	4

a - The symbol @ must precede the designation of the memory location whose contents become the effective address by indirection.

b - "k" equals the number of bits shifted.



Bit Position	Flag Name	Mnemonic	Significance
15	Link	L	Used for double-word shifts
14	Overflow	OV	Set if an arithmetic overflow occurs
13	Carry	CY	Set if a carry occurs (from most significant bit) during an arithmetic operation
12 through 0	General-Purpose Flags	GF	Use specified by user (Status flags 0 and 12 are externally available)

Figure 2-3. CPU Status Flag Assignments

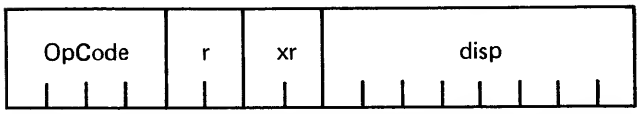


Figure 2-4. Format for Basic Memory Reference Instructions

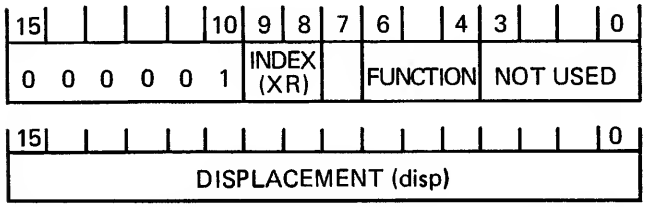


Figure 2-5. Modified Memory Reference Instruction Format

3.0 IMP-16P DESCRIPTION

The major functional units comprising the IMP-16P are shown in figure 3-1. The Central Processing Unit, Memory, and Peripheral Devices communicate and exchange data with one another by way of the four separate buses.

The layout of the IMP-16P is shown in figure 3-2. The basic configuration of the IMP-16P may be altered by the user to suit his particular requirements and may be changed by means of plug-in cards.

A programmers control panel is supplied with the IMP-16P to provide access to the CPU registers and memory. It includes an array of data switches, data and address indicators, and function switches. Using the programmers control panel, the operator may address, load, and examine CPU registers and control the operation of the microcomputer.

The IMP-16P CPU card is either the IMP-16C/200 or IMP-16C/300; therefore, the instruction sets are the same (tables 2-1 and 2-2).

IMP-16P CONFIGURATION (Figure 3-2)

One 12-connector card cage is supplied with the basic IMP-

Table 2-2. IMP-16 Extended Instruction Set

Instruction	Mnemonic	Execution Cycles
Multiply	MPY	106 to 122
Divide	DIV	125 to 159
Double Precision Add	DADD	12
Double Precision Subtract	DSUB	12
Load Byte	LDB	20 (left) 12 (right)
Store Byte	STB	24 (left) 17 (right)
Set Status Flag	SETST	17 to 36
Clear Status Flag	CLRST	17 to 36
Skip if Status Flag True	SKSTF	19 to 39
Set Bit	SETBIT	15 to 34
Clear Bit	CLRBIT	15 to 34
Complement Bit	CMPBIT	15 to 34
Skip if Bit True	SKBIT	19 to 39
Interrupt Scan	ISCAN	9 to 80
Jump Indirect to Level Zero Interrupt	JINT	7
Jump Through Pointer	JMPP	7
Jump to Subroutine Through Pointer	JSRP	8

16P microcomputer. It is prewired to accommodate the CPU, two 4K memory cards, a memory timing and control card, a control panel interface, and a TTY/card reader controller. One additional 6-connector card cage may be installed for expansion. If still more expansion is required, the power supplies may be removed and remotely installed, thus providing space for an additional pair of 6-connector card cages.

- Control panel service routines, basic loaders (for paper tape and card reader), and basic Teletype and card reader service routines are included on the interface card modules supplied as part of the basic IMP-16P.
- CPU-Module – One card constituting the CPU, bus interface logic, 256-by-16-bit RAM, and sockets for 512-by-16-bit ROM.
- Memory Module – The memory module provides 4096 16-bit words of read/write, random access semiconductor memory (RAM). The address range of a memory module is selected by backplane wiring connection. Systems may be configured with memory add-on to a maximum of 65,536 words in increments of 4096 words.

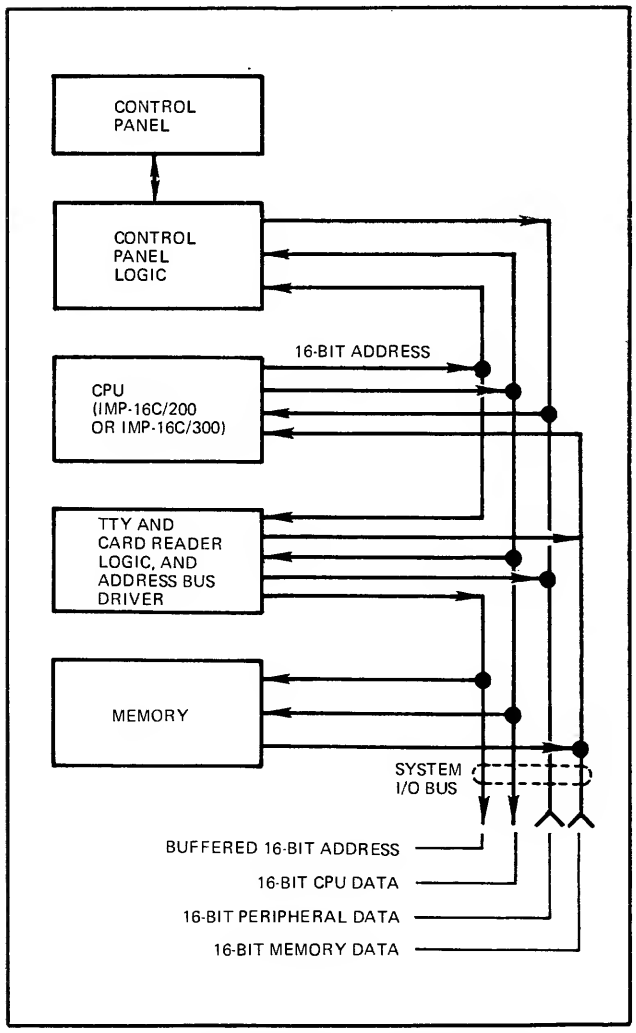


Figure 3-1. Block Diagram of Basic IMP-16P

- Interface Modules – One card containing both Teletype and card reader interfaces is included in the system, as is one card devoted to the control panel interface function.
- Prototyping Cards – Blank cards are available, drilled to accept 64 or 90 wire-wrap sockets. These cards facilitate development of interface circuits.

SYSTEM I/O BUS (Figure 3-1)

All communications between the CPU and various modules of the IMP-16P occur on the System I/O Bus. This bus consists of 16 buffered address lines, 16 memory data-in lines, 16 peripheral data-in lines, 16 memory data-out lines, and control lines (to synchronize data exchanges with the CPU).

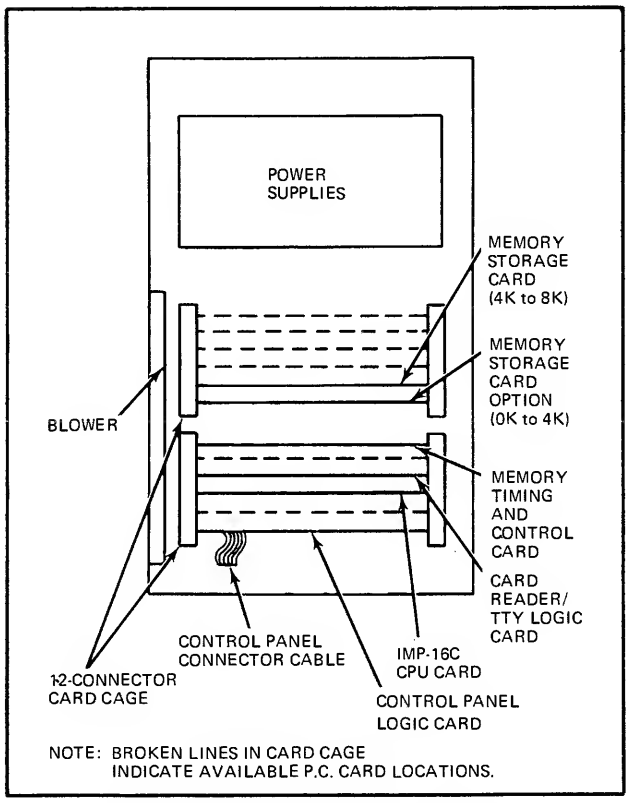


Figure 3-2. Top Internal View of IMP-16P

CONTROL PANEL

The programmers control panel offers access to the CPU registers and system memory and provides features useful in program debugging and system operation. The control panel logic module contains the interfacing circuits needed for the control panel.

PERIPHERAL UNITS

The peripheral controllers that are supplied with the IMP-16P are described below. For the OEM customer, the peripheral device, as well as the peripheral electronics

(controller), can be supplied. Detailed information is available for designing custom interfaces between the IMP-16P bus and other peripheral devices.

A Teletype bit-serial interface is supplied with the IMP-16P. This "minimum cost" interface operates under control of the CPU. Full duplex communication with a single Teletype is possible with this controller. The Card Reader Controller is on the same module as the Teletype Controller. The Card Reader Controller also operates under program control to minimize the cost of the interface logic.

IMP-16P, IMP-16C, AND OPTIONS

An assortment of hardware, firmware, and software items are available as part of and for the support of the IMP-16P microcomputers and the IMP-16C cards. These are listed in table 3-1.

Table 3-1. Major IMP-16 Units and Options

Item	Units, Contents, Options	Order Number
1	IMP-16P Microcomputer System HARDWARE: • Chassis (wired for the following: 8K memory, card reader and TTY controller, memory timing and control card, control panel interface, and CPU. • Power Supply Assembly • IMP-16C/200 CPU Card (includes one CROM on IMP-16C/200, socket for second CROM or second CROM on IMP-16C/300, and eight sockets for PROMs or ROMs – MM5203 or MM5213 or available firmware) • 4096-word Read/Write Memory Card • Memory Timing and Control Card • TTY/Card Reader Controller Card and Connectors • 12-Connector Card Cage • Programmers Control Panel • IMP-16C Application Method REFERENCE MANUALS: • IMP-16P Users Manual • IMP-16 Programming and Assembler Manual • IMP-16 Utilities Reference Manual • Tymshare Users Manual SOFTWARE: • IMP-16P Software Debug Routine • Self-Assembler • Diagnostic Programs FIRMWARE: • Control Panel Service Routines • Basic Loaders (Paper Tape & Card Reader) • Basic Teletype and Card Reader Service Routines	IMP-16P/yxx NOTE The IMP-16P is available with one or more 4K RAM memory modules, as IMP-16P/yxx. "xx" is the approximate number of thousands of memory words included with the system. Thus, an an 8K system would be designated IMP-16P/y08. "y" is "2" if the system uses an IMP-16C/200 CPU card (no extended instruction), or is a "3" if the system includes an IMP-16C/300 CPU card (has extended instruction set).
2	IMP-16C/200 or IMP-16C/300 Microprocessor Card • IMP-16 Programming and Assembler Manual • Tymshare Users Manual • IMP-16C Application Manual • IMP-16C Interfacing Guide	IMP-16C/200 or IMP-16C/300

Table 3-1. Major IMP-16 Units and Options (continued)

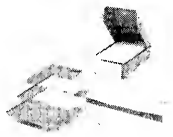
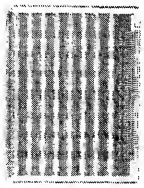
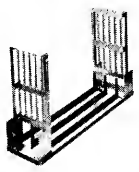
Item	Units, Contents, Options	Order Number
	OPTIONS	
3	ROM Diagnostic Program (ROMDI) • 4-ROM set for verifying CPU operation	IMP-16F/501
4	ROM Utility Program (CUTIL) – for IMP-16C only • Contains TTY, control panel, and binary paper tape punch routines (2 ROMs)	IMP-16F/000
5	ROM Program Debugging Routine (DEBUGC) – for IMP-16C only • Use with CUTIL for simple debugging aid (2 ROMs)	IMP-16F/002
6	ROM Utility Program (CMEMDI) – for IMP-16C only • Memory diagnostic, control panel, and demonstration programs (2 ROMs)	IMP-16F/500
7	IMP-16 Assembler (Cross Assembler written in FORTRAN) • Source deck • Listing • IMP-16 Programming and Assembler Manual • Card Decks with listings for format conversion routines	IMP-16S/900A 
8	Card Reader (Documation Model M300L – 300 cards per minute)	IMP-00/825
9	Teletype (ASR Model 33)	IMP-00/810
10	4K Memory Card (RAM)	IMP-16P/004
11	Memory Timing and Interface Control Card (will control up to eight IMP-16P/004 Memory Modules)	IMP-16P/004T 
12	Prototyping Card – 64-socket blank circuit card for use with wire-wrapped sockets (sockets not included)	IMP-00H/891 
13	Prototyping Card – 90-socket blank circuit card for use with wire-wrapped sockets (sockets not included)	IMP-00H/892 

Table 3-1. Major IMP-16 Units and Options (continued)

Item	Units, Contents, Options	Order Number
	OPTIONS	
14	Card Extender	IMP-00H/890 
15	3-Card Connector Panel: Card frame with three 144-pin wire-wrap connectors and card guides, spaced to accommodate wire-wrap Prototyping Cards.	IMP-00H/881 
16	6-Card Connector Panel: Card frame as above but with six 144-pin wire-wrap connectors and card guides, spaced to accommodate PC cards.	IMP-00H/880 

4.0 SOFTWARE

ASSEMBLER

An assembler written in ANSI FORTRAN is available. This allows maximum transferability to a wide variety of large computer systems and the advantage of file management and text editing capabilities of large general-purpose computer systems.

The assembler contains the following features:

- Relocatable- or absolute-load-module generation
- Conditional assembly features
- Global symbols for communication between independent assemblies
- Wide variety of assembly-time operators (+, –, *, /, AND, OR, NOT)
- Local symbols
- Error messages including error position in the source line

Utility programs written in ANSI FORTRAN are available for conversion of the assembler object output to various media (for example, punched cards and paper tape) and various formats.

The assembler with its supporting utility programs has been installed on a nationwide computer utility (timesharing) service and thus is readily available to a wide range of users.

DIAGNOSTIC PROGRAMS

Extensive diagnostic programs are available for testing and verifying operation of both the central processing unit and the memory.

LOADERS

A variety of loaders is available for entering programs produced by the assembler into read/write memory. The input media may be either punched cards or paper tape. The format of the programs may be either absolute or relocatable modules.

The following loaders are provided:

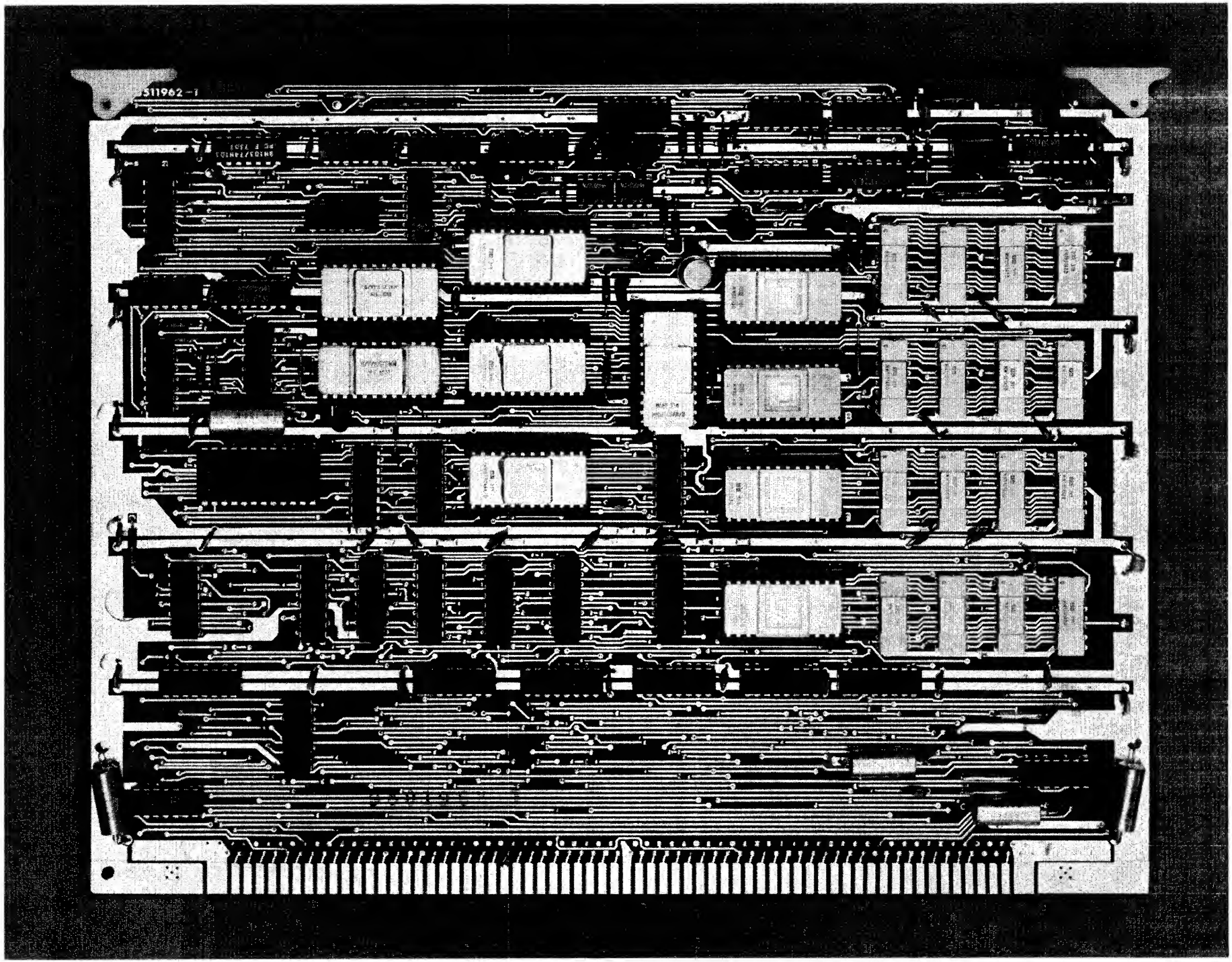
- A firmware paper tape loader, which can be activated by the LOAD PROG switch on the control panel and which loads an absolute program module via the paper tape reader
- A card reader loader (implemented with firmware), which loads one or more absolute program modules via the card reader

- A relocating, linking loader, which loads one or more program modules via the card reader or paper tape, relocates them to any location in memory, and links them together via global symbols specified at assembly time

PROGRAM DEBUG AID

DEBUG is a relocatable object program that provides aids for the efficient development of user's programs. The program is designed to be used with a Teletypewriter to allow the operator to perform the following debugging functions:

- Printing the contents of registers or selected areas of memory
- Modifying the contents of registers or memory locations
- Providing instruction breakpoint halts or "snapshots" during the execution of a user's program
- Allowing the initiating of execution at any point in a program
- Searching memory



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